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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/746,823	12/22/2000	Erik Bengtsson	8194-453IP	8910

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EXAMINER	
TRAN, KHANH C	

ART UNIT	PAPER NUMBER
2631	10

DATE MAILED: 07/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/746,823	BENGTSSON ET AL.	
	Examiner	Art Unit	
	Khanh Tran	2631	

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,16-30 and 34-36* is/are rejected.

7)☒ Claim(s) *13-15 and 31-33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The Amendment filed on 04/21/2004 has been entered. Claims 1-36 are pending in this Office action.

Response to Arguments

2. The rejections of claims 1-9 and 20-27 have been withdrawn in light of Applicants invoking 35 U.S.C 103(c) applying to the pending application.

3. Applicant's arguments with respect to claims 1-36 have been considered but are moot in view of the new ground(s) of rejection.

4. The amended abstract has been accepted.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-12, 16-27, 28-30, and 34-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gailus et al. U.S Patent 6,449,465 B1.

Regarding claim 1, as disclosed in column 5 line 7 through column 6 line 36, figure 4 illustrates a linear transmitter 306 including:

- a digital signal processor (DSP) 401 that generates a digital baseband signal comprising an in-phase (I) component 404 and a quadrature (Q) component 403. The DSP 401 further generates an amplitude component 402;
- an input phase modulator 424, preferably a voltage controlled oscillator (VCO) synthesizer, a feedback circuit 416 coupled to the input phase modulator 424 and DSP 401, wherein the VCO inherently has an output, and the feedback circuit 416 includes an I/Q modulator. Gailus et al. does not expressly disclose a phase locked loop (PLL) having features as claimed in the pending application. However, the VCO synthesizer includes a controlled voltage oscillator having an output as claimed and the feedback circuit 416 includes an I/Q modulator as claimed and a comparator 502 (see figure 5). In light of the aforementioned, it would have been obvious for one of ordinary skill in the art at the time the invention was made that the combination of input phase modulator 424 and feedback circuit 416 forms a PLL having features as claimed in the pending application because the combination has all the features of a conventional PLL as decribed above. Furthermore, Gailus et al. discloses in column 5 lines 45-51 that input phase modulator 424 might

alternatively be any kind of frequency reference with dividers and feedback loop.

- an amplifier PA 410 (see figure 4) having an input, an output, and amplitude control input coupled through a switching power supply 426, wherein PA 410 receives an input signal 411 responsive to the VCO output of the input phase modulator 424 and the amplitude control input is responsive to the amplitude signal through the switching power supply 426.

Regarding claims 2 and 21, figure 7 illustrates an alternate embodiment of the feedback circuit portion. As recited in claim 1, a PLL is in the form of the input phase modulator 424 and the feedback circuit 416. The PLL includes a controlled oscillator input 422, the feedback circuit 416 between the controlled oscillator input 422 and the controlled oscillator output 411, wherein the feedback circuit 416 includes a mixer 710 responsive to a local oscillator 742, and wherein the I/Q modulator is between the mixer 740 and controlled oscillator input 422.

Regarding claims 3 and 22, as disclosed in column 5 lines 52 through column 6 line 11, DSP 401 also converts the quadrature modulation information signal to a polar format. Those skilled in the art will appreciate that the polar conversion process would normalize the in-phase and quadrature-phase signals, and the modulated signal is a constant amplitude modulated signal as claimed in the pending application.

Regarding claims 4 and 23, as shown in figure 5, in-phase and quadrature-phase signals are applied to the I/Q modulator 506 wherein the modulator 506 applies a cosine of the phase value theta to a cosine modulator 526, and a sine of the phase value theta to a sine modulator 524, and where the phase value theta is an angle whose tangent is the quadrature phase signal divided by the in-phase signal as appreciated by one of ordinary skill in the art.

Regarding claims 5 and 24, those skilled in the art will appreciate that the amplitude signal is a square root of a sum of the in-phase signal squared and the quadrature-phase signal squared.

Regarding claims 6 and 25, figure 4 shows a power control signal through a switching power supply 426, wherein the amplitude control input of PA 410 is responsive to the power control signal and to the amplitude signal 407 through switching power supply 426 as appreciated by one of ordinary skill in the art.

Regarding claims 7 and 26, Gailus et al. does not expressly disclose employment an amplifier in conjunction with a power amplifier. Nevertheless, one of ordinary skill in the art will appreciate that such implementation is well known in the art and is just a design choice. The linear transmitter in figure 4 inherently includes a transmit antenna responsive to the output of PA 410 through impedance modulator 412.

Regarding claims 8 and 27, figure 4 does not show a transmit antenna. Nevertheless, the linear transmitter in figure 4 inherently includes a transmit antenna responsive to the output of PA 410 through impedance modulator 412. Figure 4 does not show a user interface as claimed. However, one of ordinary skill in the art will appreciate that the DSP 401 is responsive to a user interface that generates a baseband signal in response to a user input as claimed in the patent application.

Regarding claim 9, the PA 410 in figure 4 is a power amplifier.

Regarding claim 10, referring to figures 4 and 5 again, as disclosed in column 5 line 7 through column 6 line 36, figure 4 illustrates a linear transmitter 306 including:

- a feedback circuit 416 having I/Q modulator 506 that modulates in-phase signal 409 and quadrature-phase signal 408 to produce a modulated signal 530.
- Gailus et al. does not expressly disclose a phase tracking subsystem as claimed. Nevertheless, a phase modulation error signal 422 is produced in responsive to the modulated signal 530 through a second downconverter mixer 516, splitter 518, and comparator 502. The phase modulation error signal 422 is independent of amplitude changes in the modulated signal as appreciated by one of ordinary skill in the art. Using the same argument as claim 1, a PLL is in the form of the combination of input phase modulator 424 and feedback circuit 416. In light of the

foregoing, it would have been obvious for one of ordinary skill in the art at the time the invention was made that second downconverter mixer 516, splitter 518, comparator 502, I/Q modulator 506, and input phase modulator 424 would form a phase subsystem having similar components and performing equivalent functions as set forth in the claimed invention.

- Similarly, an amplified amplitude modulation error signal 420 is produced in responsive to the modulated signal 530 through a first downconverter mixer 514. The amplitude modulation error signal 420 is independent of phase changes in the modulated signal as appreciated by one of ordinary skill in the art. Using the same argument above, it would have been obvious for one of ordinary skill in the art at the time the invention was made that the amplitude tracking subsystem as claimed is in the form of the first downconverter mixer 514 and amplifier 504.
- In column 9 line 55 through column 10 line 8, in another embodiment, a modulating amplifier 428 consisting of a power amplifier 410 having an input, an amplitude control input through switching power supply 426, and an output to a signal coupler 414, wherein the input is responsive to the phase signal 411, the amplitude control input is responsive to the amplitude modulation error signal 420.

Regarding claim 11, said claim is rejected on the same ground as claim 2.

Regarding claim 12, Gailus et al. does not expressly disclose an automatic gain control subsystem. However, the amplitude modulation error signal 420 is amplified by an amplifier 504 to produce an amplified amplitude modulation error signal 420. In light of the foregoing, the amplifier 504 inherently provides an automatic gain control and is part of the amplitude tracking subsystem as claimed in the pending application.

Regarding claim 16, figure 5 discloses a limiter 520 coupled between the I/Q modulator 506 and the formed PLL.

Regarding claim 17, said claim is rejected on the same ground as claim 7.

Regarding claim 18, said claim is rejected on the same ground as claim 8.

Regarding claim 19, said claim is rejected on the same ground as claim 9.

Regarding claim 20, said claim is rejected on the same ground as claim 1 because the claim claims a method performing the steps in claim 1.

Regarding claim 28, said claim is rejected on the same ground as claim 10.

Regarding claim 29, said claim is rejected on the same ground as claim 11.

Regarding claim 30, said claim is rejected on the same ground as claim 12.

Regarding claim 34, said claim is rejected on the same ground as claim 16.

Regarding claim 35, said claim is rejected on the same ground as claim 17.

Regarding claim 36, said claim is rejected on the same ground as claim 18.

Allowable Subject Matter

6. Claims 13-15, and 31-33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Edwards et al. U.S. Patent 6,415,002 B1 discloses "Phase and Amplitude Modulation of Baseband Signals".

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 703-305-2384. The examiner can normally be reached on Tuesday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 703-306-3034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KCT

JEAN B. CORRIELUS
PRIMARY EXAMINER
7/8/04